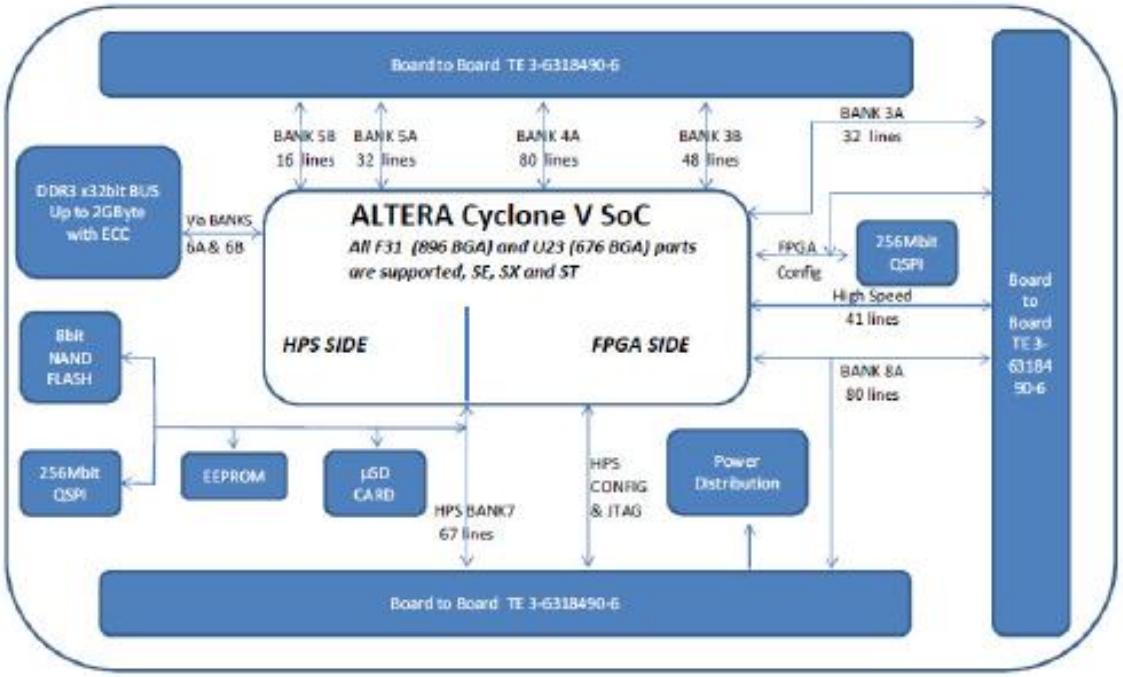
LLRF Hardware Platform based on System on Module(SOM) FPGA

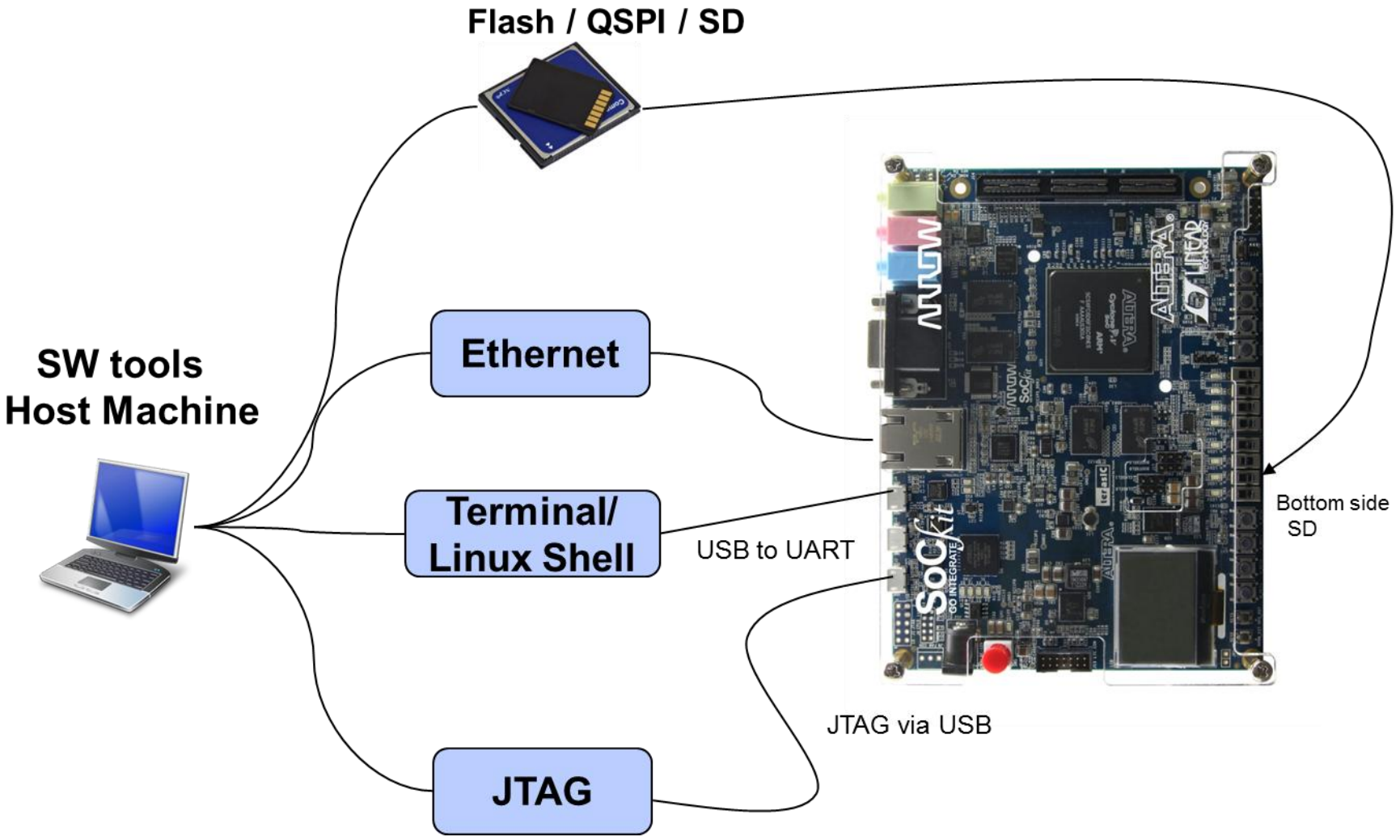
P. Varghese

System on a Module (SOM)

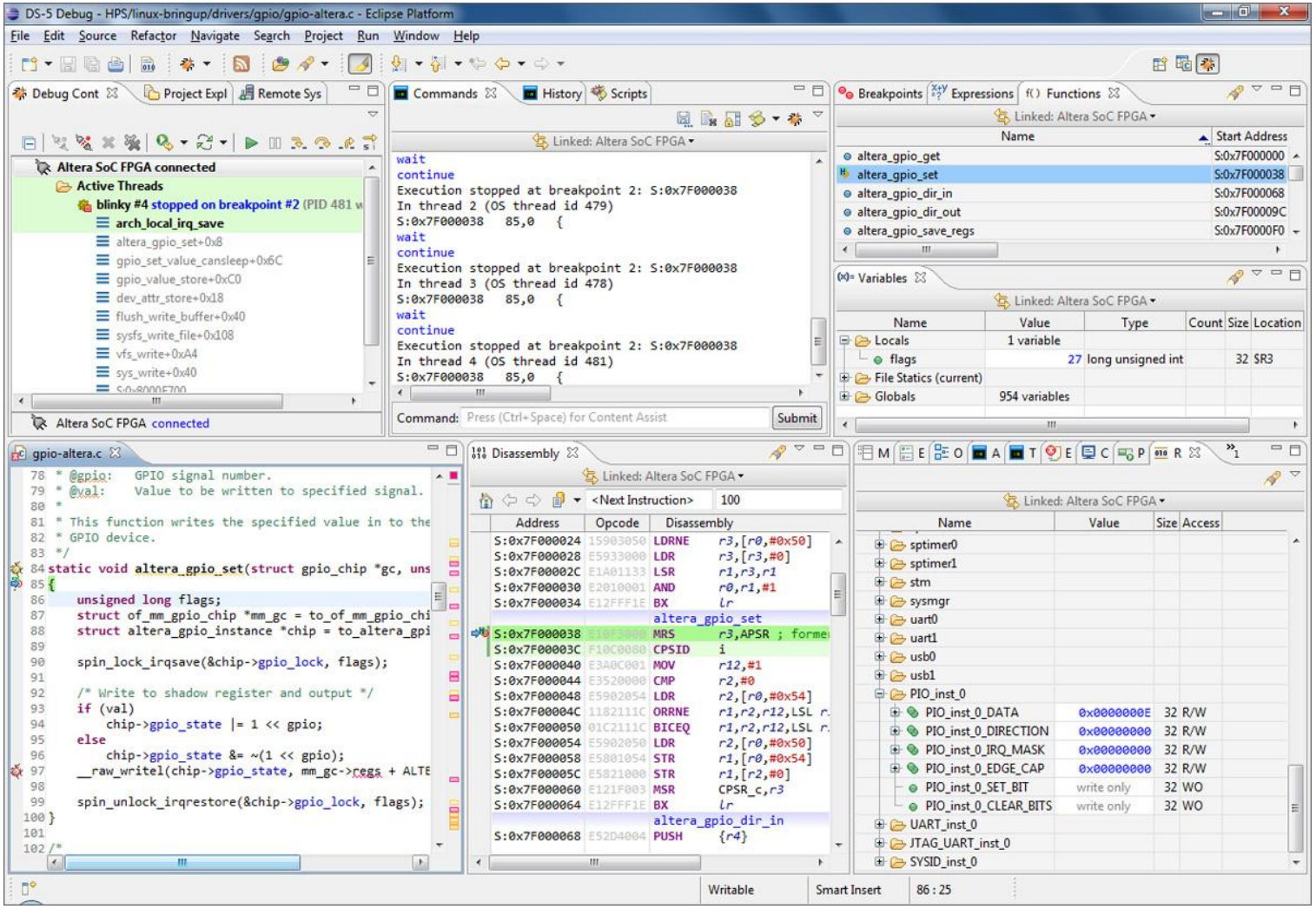


- 2Gbyte DDR3
- 64Mbyte QSPI FLASH for HPS boot
- µSD slot connected to HPS
- 64Mbyte QSPI FLASH for FPGA boot
- Three Board to Board connectors, 220 Pins each
- Carrier Board has mating connector, TYCO TE 318272536

Debug Interfaces

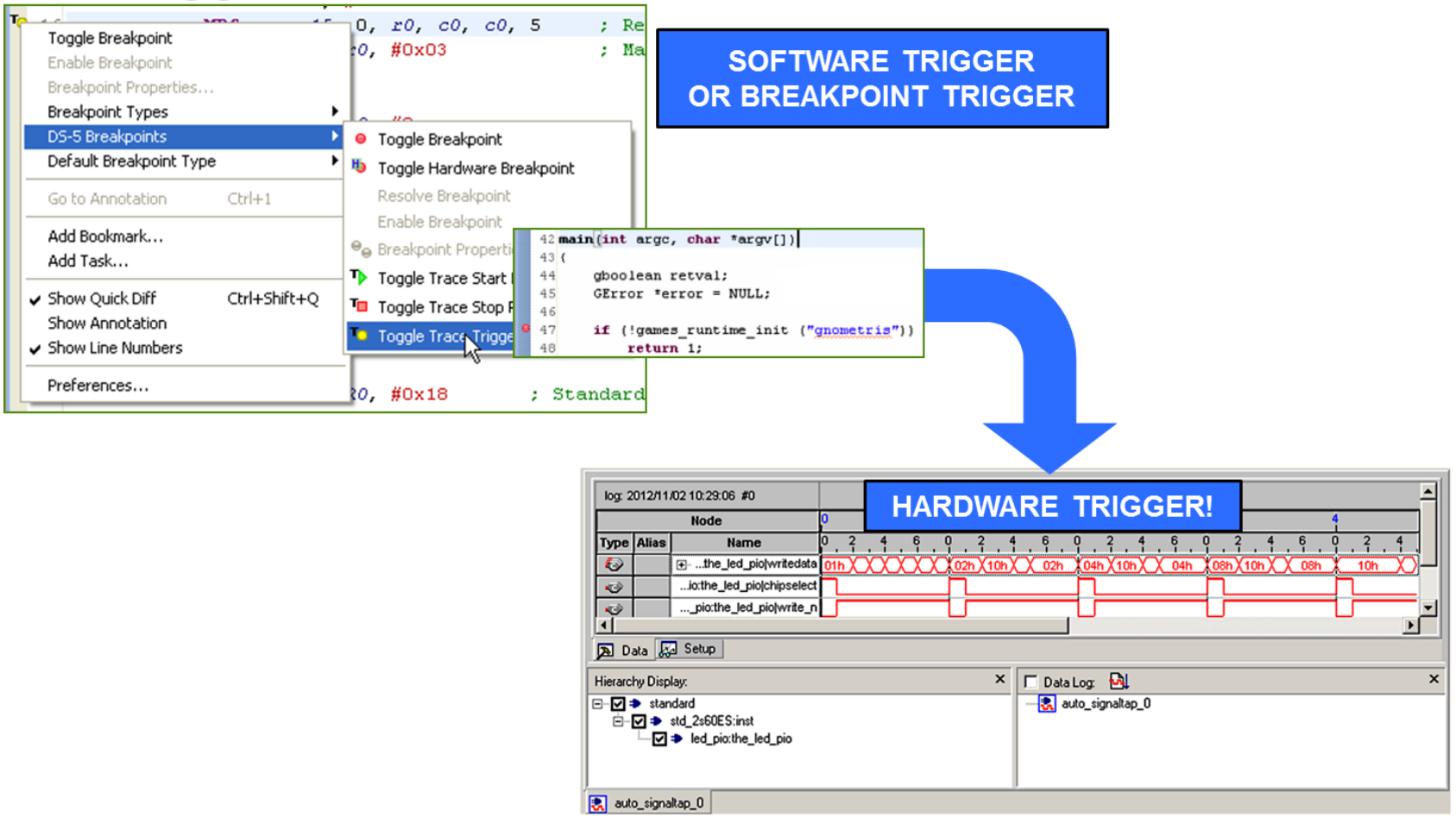


DS-5 Debugger for ARM

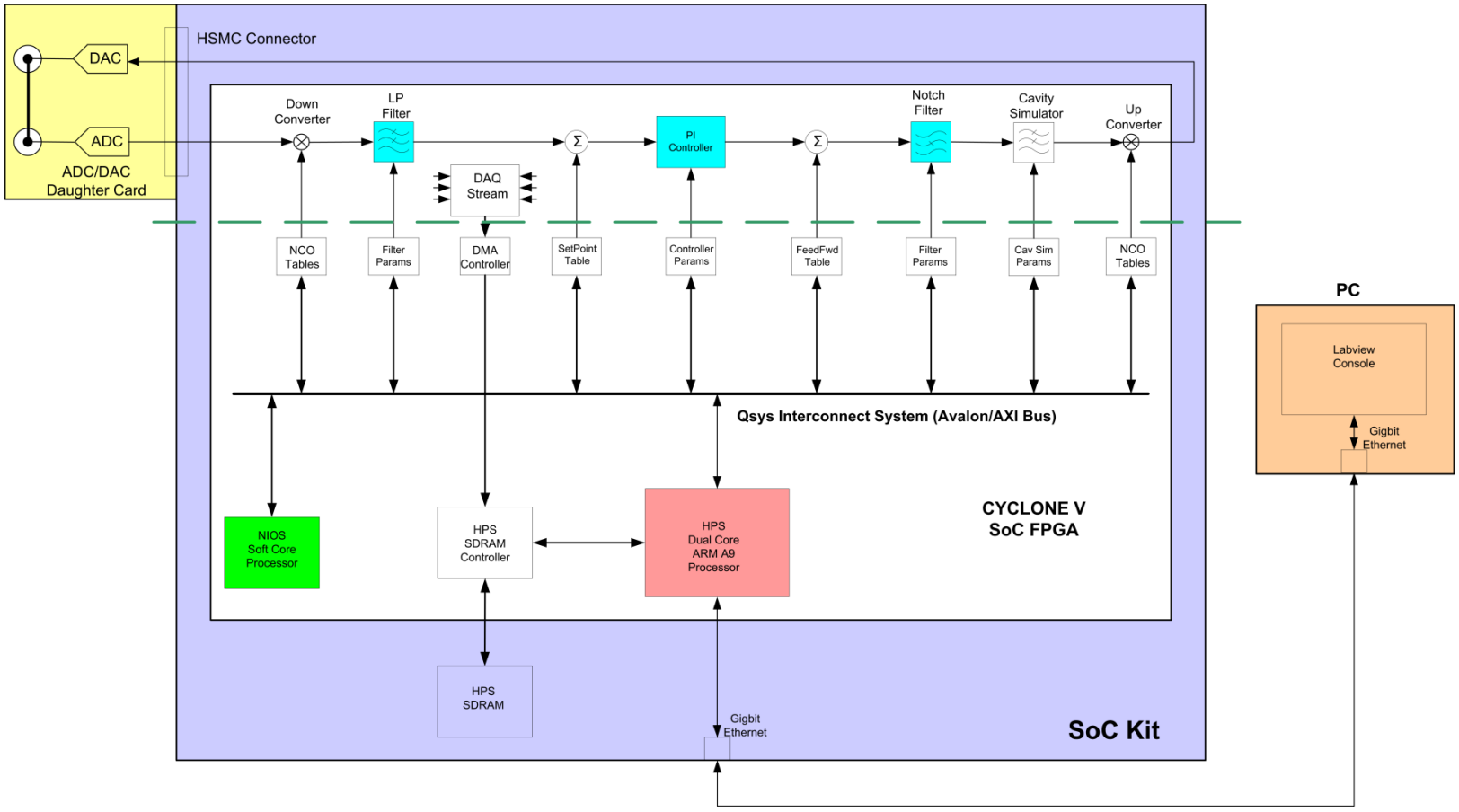


Cross Domain Debug1

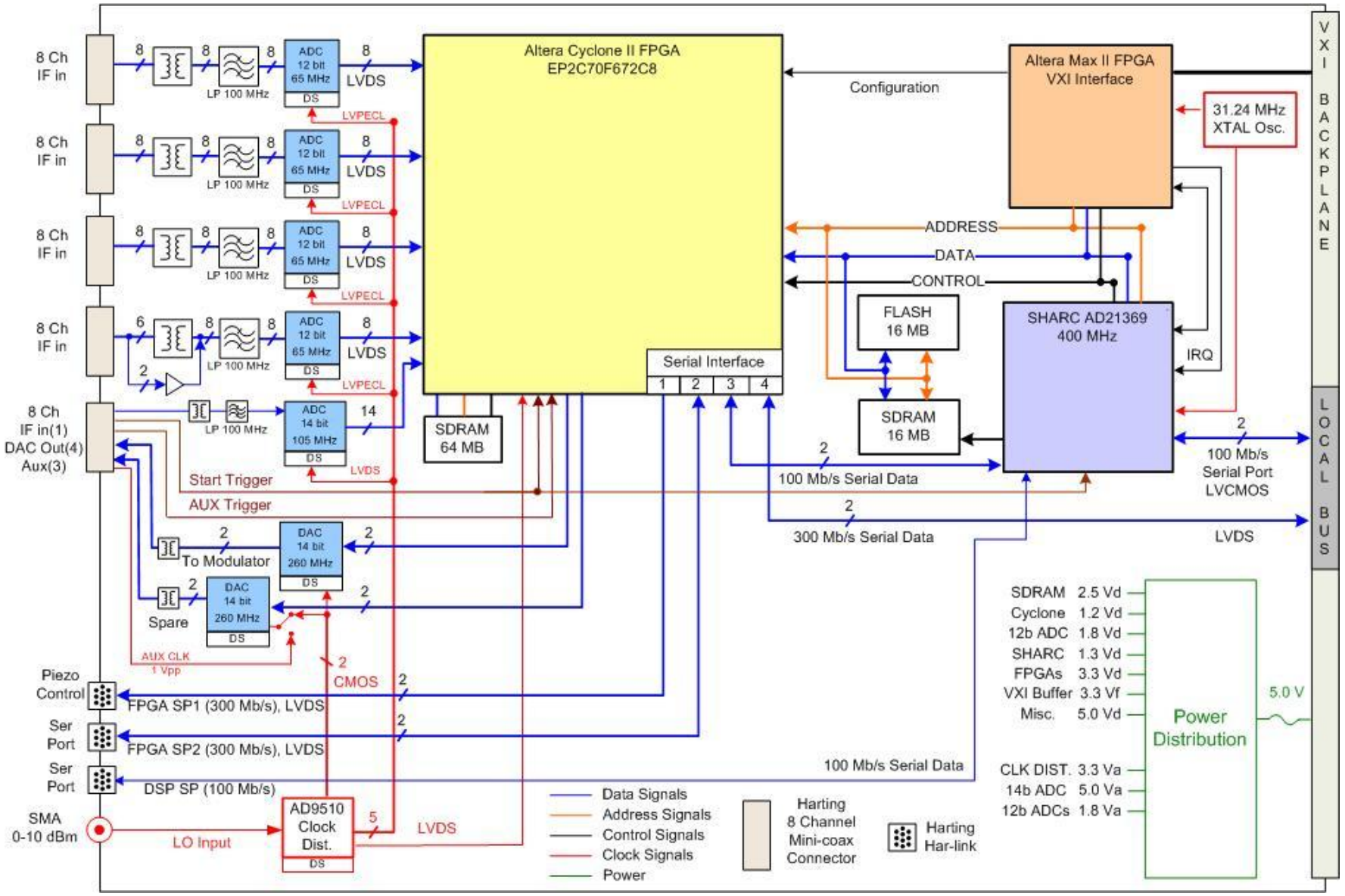
- Trigger from software to FPGA



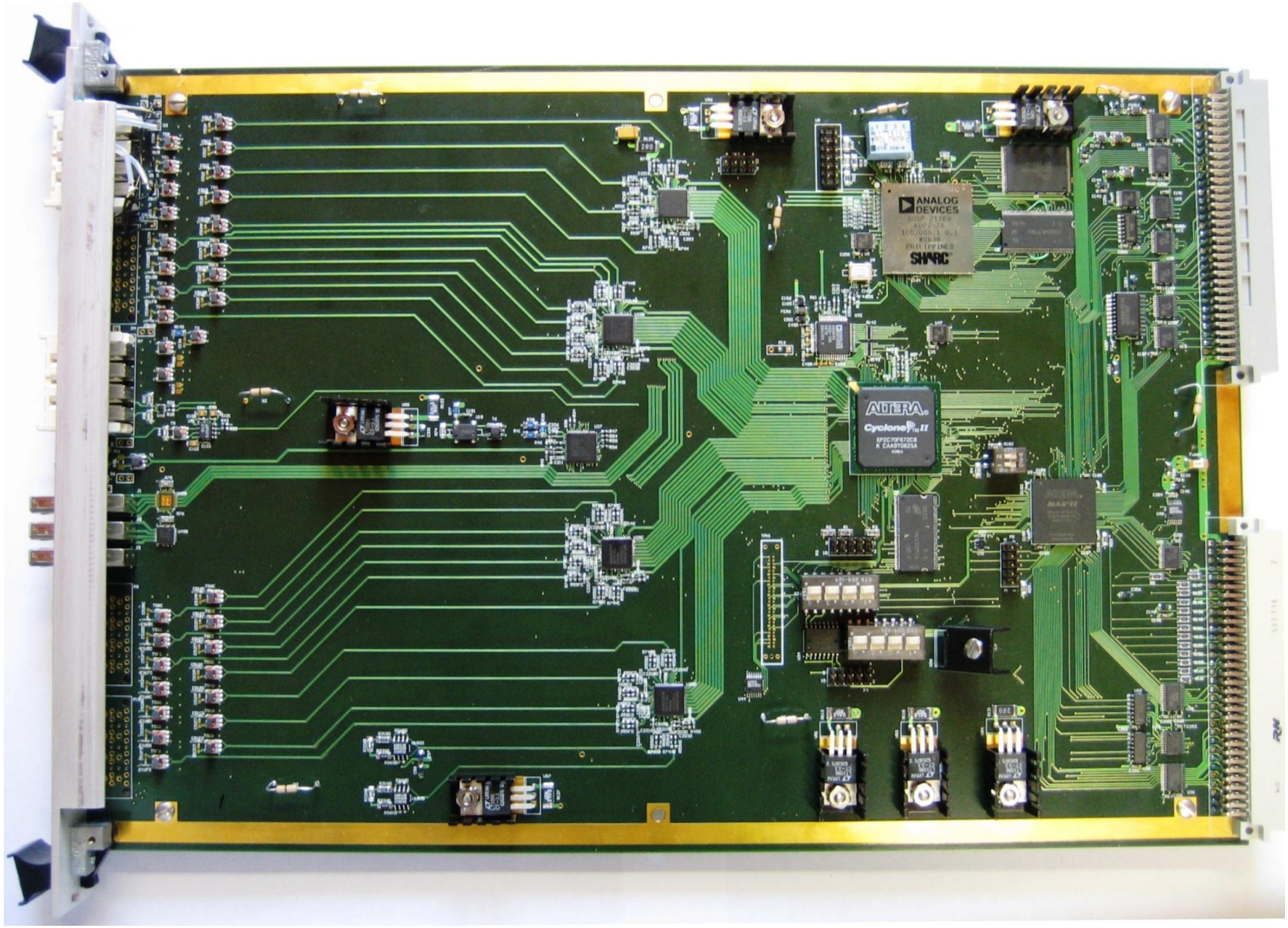
LLRF System Example



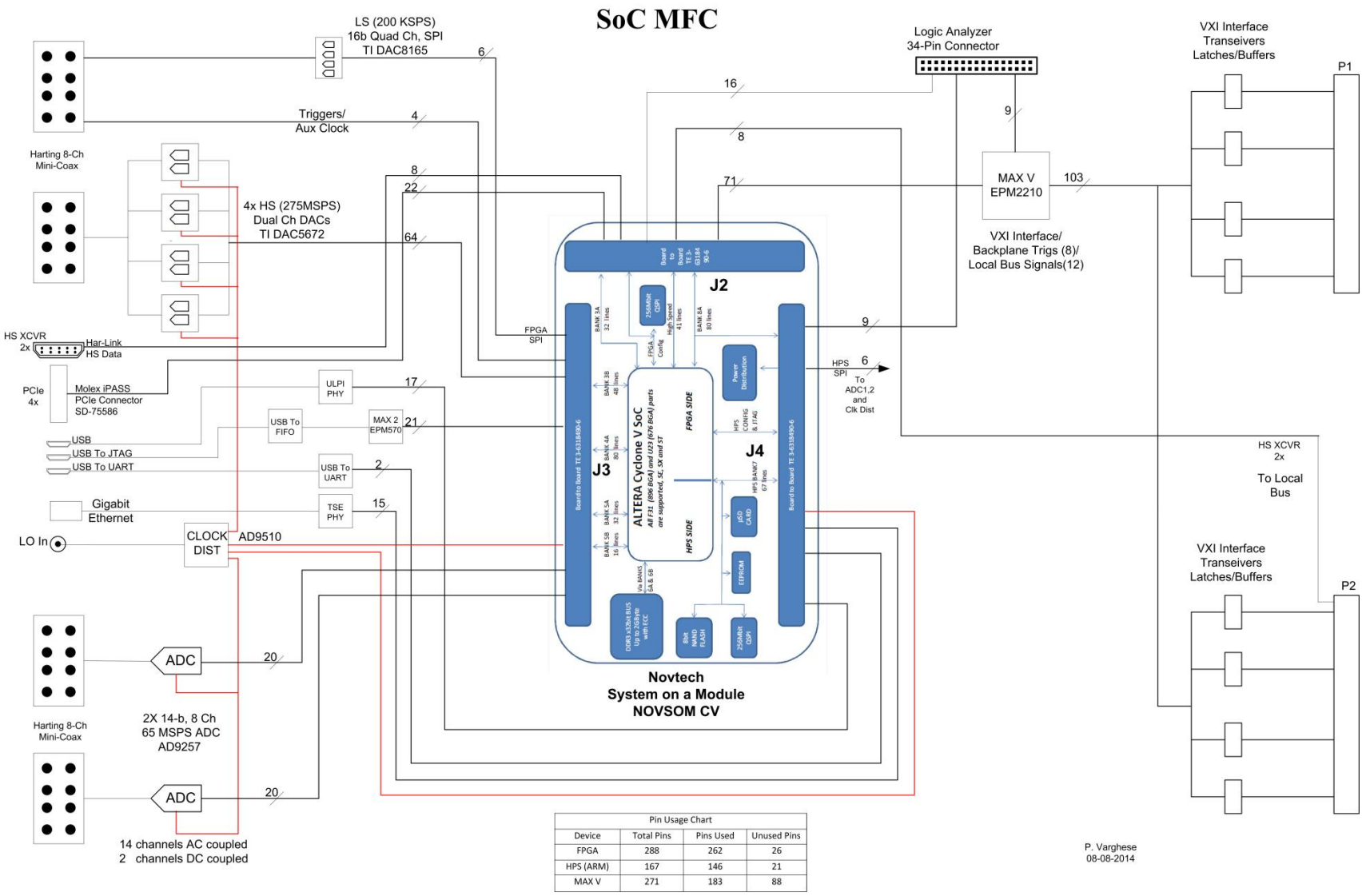
Cyclone II based MFC (2007)



33 ADC ch, 4 DAC ch



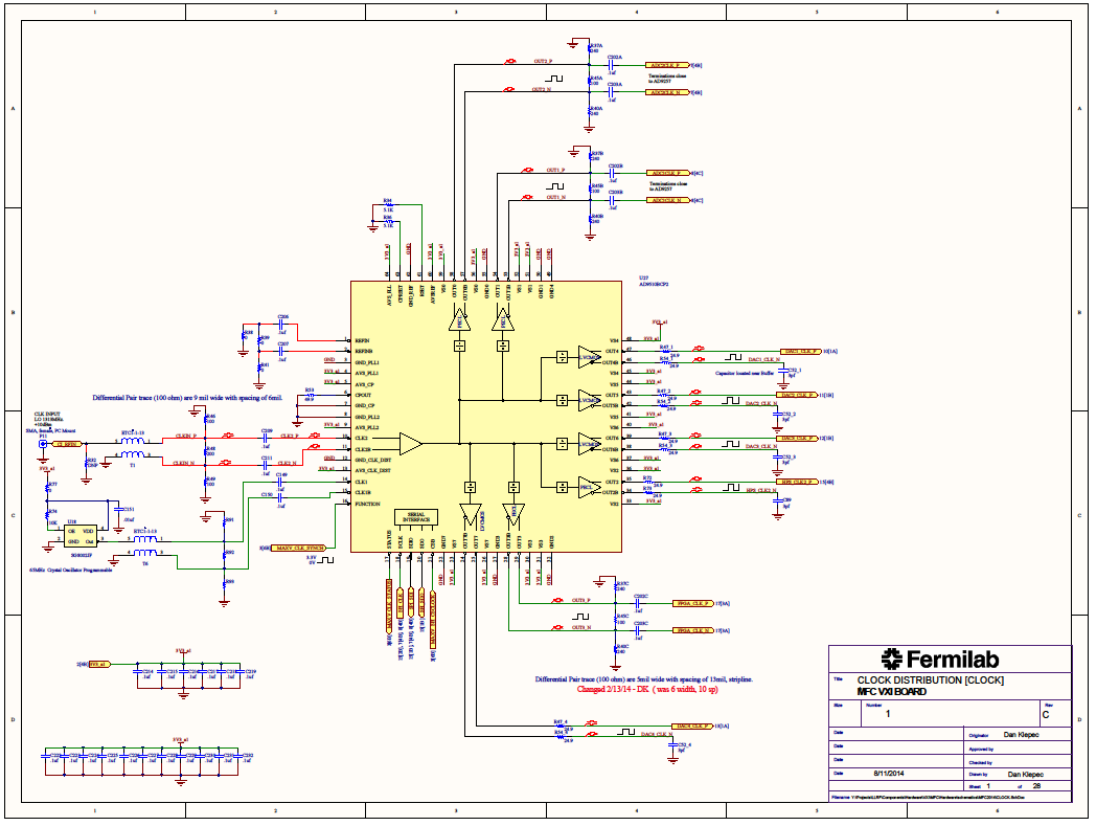
SoC Cyclone V SOM based MFC (2014)



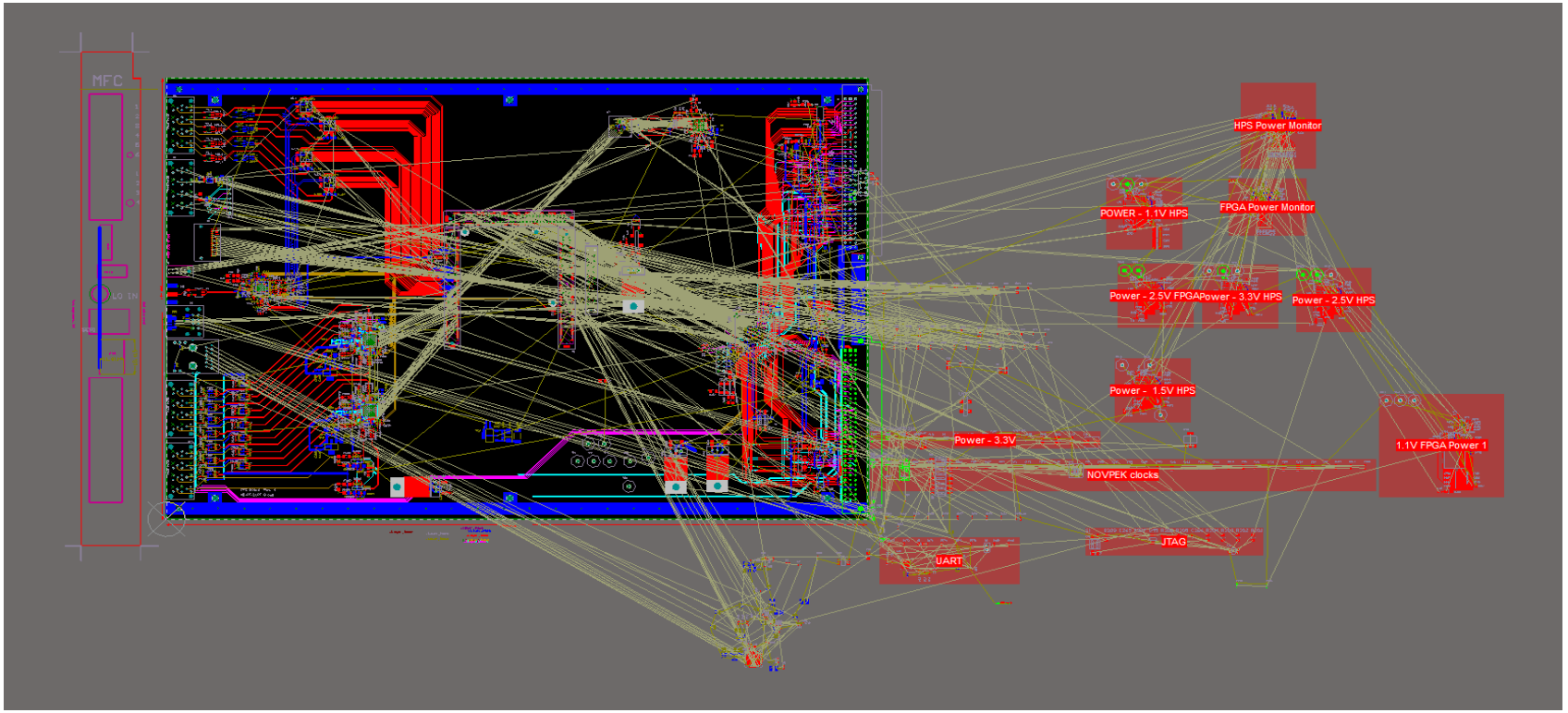
Pin Usage Chart			
Device	Total Pins	Pins Used	Unused Pins
FPGA	288	262	26
HPS (ARM)	167	146	21
MAX V	271	183	88

P. Varghese
08-08-2014

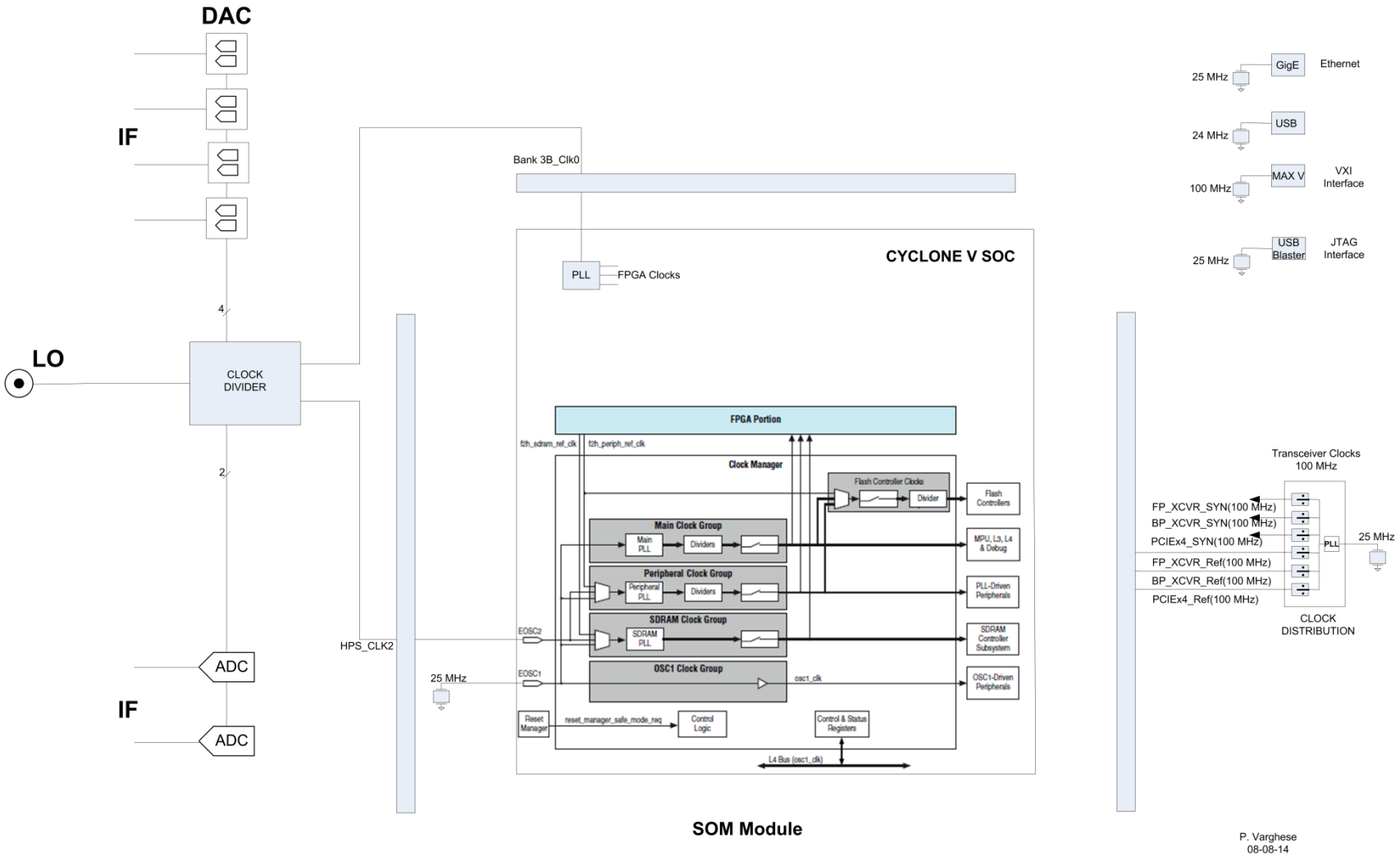
Schematics Completed



Layout ~ 2/3 Completed



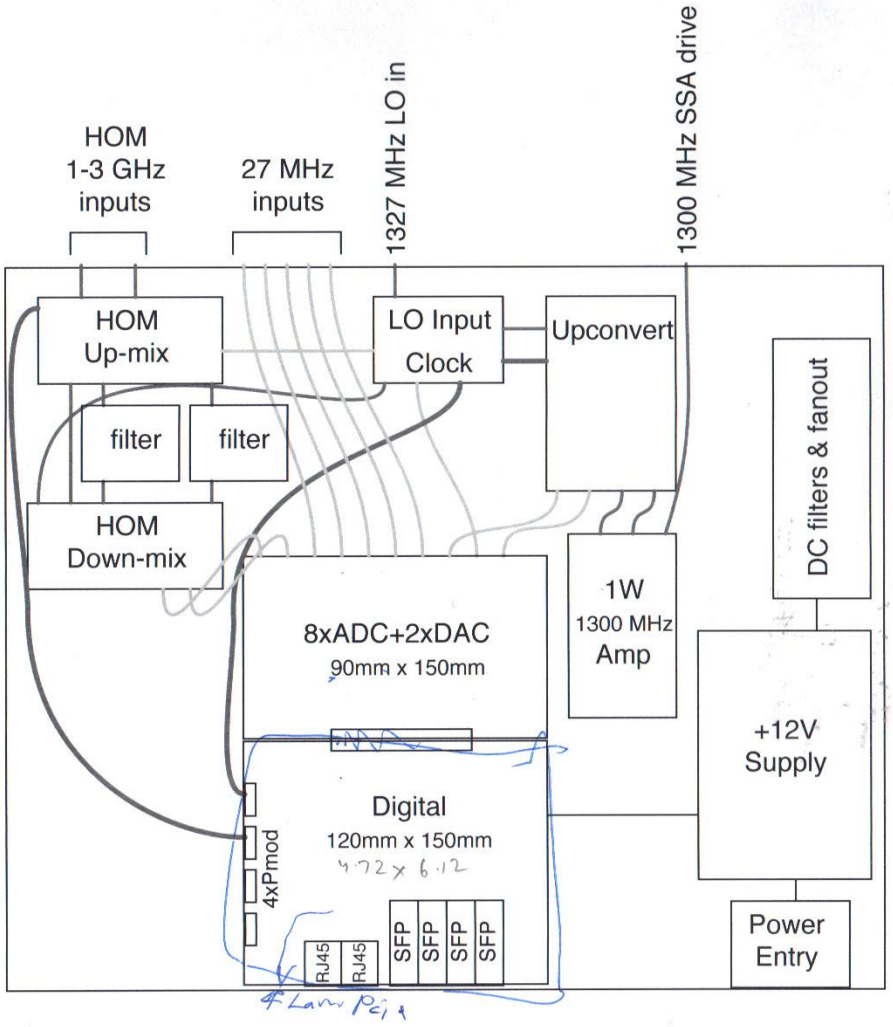
SoC MFC Clock Domains



SOM Module

P. Varghese
08-08-14

Cavity Controller



1U 19" chassis

17" x 14"

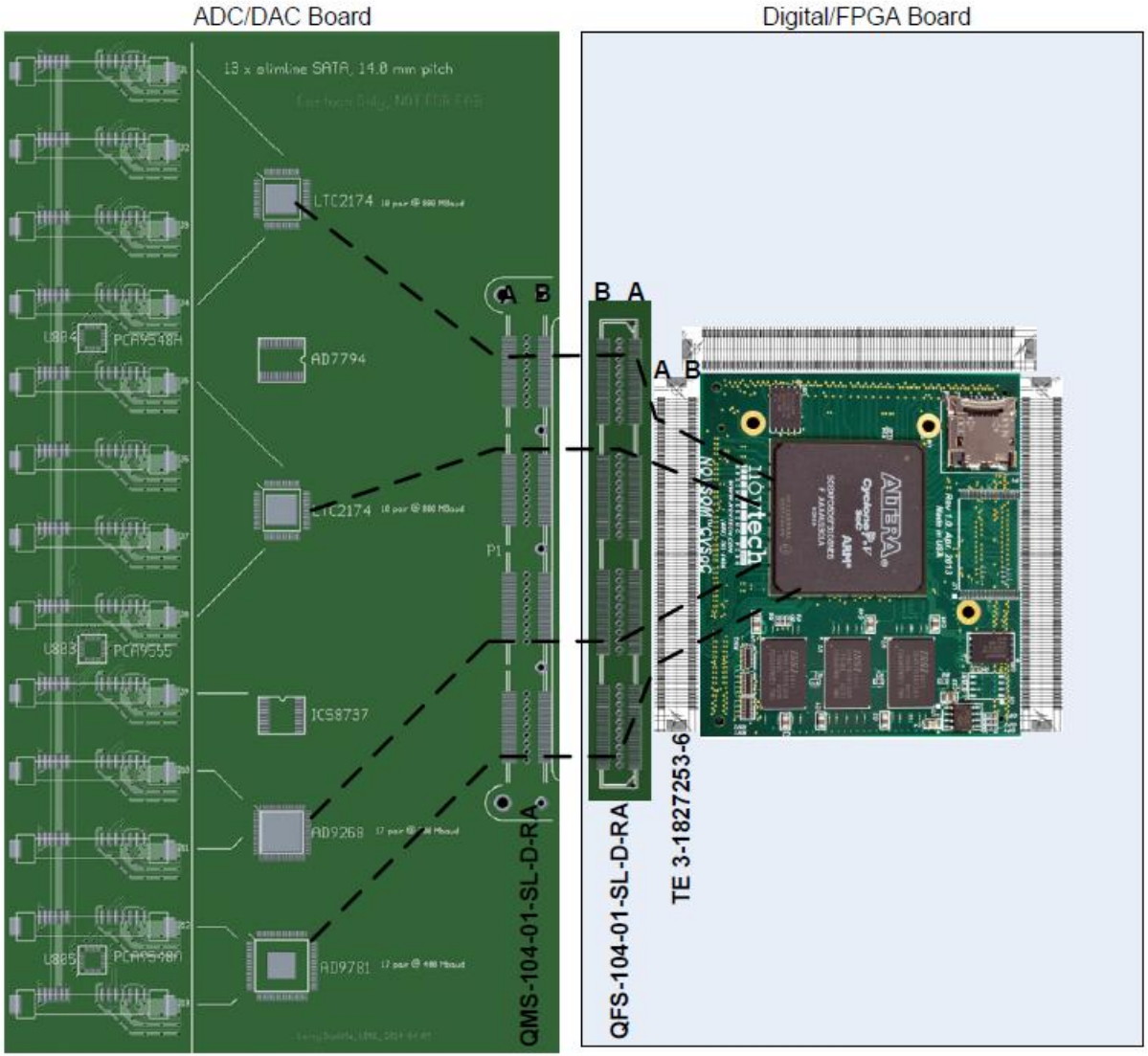
0.25" Al plate 2.6 kg

Passively cooled ~30W

Coax >1GHz

Coax <1GHz

Pmod ribbon


ADC/DAC Board
Digital/FPGA Board
18 x slimline SATA, 14.8 mm pitch
LTC2174
AD7794
LTC2174
PCA9548H
PCA9555
ICS8737
AD9268
AD9781
P1
A B
B A
A B
QMS-104-01-SL-D-RA
QFS-104-01-SL-D-RA
TE 3-1827253-6

ADC/DAC Pin Assignments

QMS-104 (ADC Brd)	QFS-104 (FPGA Brd)
A1 SCL	FPGA_SCL
A2 GND	
A3 SDA	FPGA_SDA
A4 VAUX	FPGA_3.3V
A5 GND	
A6 W01A	LTC2174_1_OUT1A_P
A7 W01B	LTC2174_1_OUT1A_N
A8 GND	
A9 W02A	LTC2174_1_OUT2A_P
A10 W02B	LTC2174_1_OUT2A_N
A11 GND	
A12 W03A	LTC2174_1_DCO_P
A13 W03B	LTC2174_1_DCO_N
A14 GND	
A15 W04A	LTC2174_1_OUT3A_P
A16 W04B	LTC2174_1_OUT3A_N
A17 GND	
A18 W05A	LTC2174_1_OUT4A_P
A19 W05B	LTC2174_1_OUT4A_N
A20 GND	
A21 W06A	LTC2174_2_OUT1A_P
A22 W06B	LTC2174_2_OUT1A_N
A23 GND	
A24 W07A	LTC2174_2_OUT2A_P
A25 W07B	LTC2174_2_OUT2A_N
A26 GND	
C1 VIO	FPGA_2.5V
C2 GND	
C3 W15A	LTC2174_2_DCO_P
C4 W15B	LTC2174_2_DCO_N
C5 GND	
C6 W16A	LTC2174_2_OUT3A_P
C7 W16B	LTC2174_2_OUT3A_N
C8 GND	
C9 W17A	LTC2174_2_OUT4A_P
C10 W17B	LTC2174_2_OUT4A_N
C11 GND	
C12 W18A	FPGA_SPI_SDO
C13 W18B	FPGA_SPI_SDI
C14 GND	
C15 W19A	FPGA_SPI_CLK
C16 W19B	
C17 GND	
C18 W20A	CLK_P

QMS-104 (ADC Brd)	QFS-104 (FPGA Brd)
B1 GND	
B2 VBULK	FPGA_5.0V
B3 VBULK	FPGA_5.0V
B4 GND	
B5 W08A	LTC2174_1_OUT1B_P
B6 W08B	LTC2174_1_OUT1B_N
B7 GND	
B8 W09A	LTC2174_1_OUT2B_P
B9 W09B	LTC2174_1_OUT2B_N
B10 GND	
B11 W10A	LTC2174_1_FR_P
B12 W10B	LTC2174_1_FR_N
B13 GND	
B14 W11A	LTC2174_1_OUT3B_P
B15 W11B	LTC2174_1_OUT3B_N
B16 GND	
B17 W12A	LTC2174_1_OUT4B_P
B18 W12B	LTC2174_1_OUT4B_N
B19 GND	
B20 W13A	LTC2174_2_OUT1B_P
B21 W13B	LTC2174_2_OUT1B_N
B22 GND	
B23 W14A	LTC2174_2_OUT2B_P
B24 W14B	LTC2174_2_OUT2B_N
B25 GND	
B26 VIO	FPGA_2.5V
D1 GND	
D2 W23A	LTC2174_2_FR_P
D3 W23B	LTC2174_2_FR_N
D4 GND	
D5 W24A	LTC2174_2_OUT3B_P
D6 W24B	LTC2174_2_OUT3B_N
D7 GND	
D8 W25A	LTC2174_2_OUT4B_P
D9 W25B	LTC2174_2_OUT4B_N
D10 GND	
D11 W26A	LTC2174_1_SPI_CS
D12 W26B	LTC2174_2_SPI_CS
D13 GND	
D14 W27A	AD9268_SPI_CS
D15 W27B	AD9781_SPI_CS
D16 GND	
D17 W28A	
D18 W28B	

C19 W20B	CLK_N
C20 GND	
C21 W21A	
C22 W21B	
C23 GND	
C24 W22A	AD9268_D0_N
C25 W22B	AD9268_D0_P
C26 GND	
E1 W00E	
E2 GND	
E3 W31A	AD9268_D2_N
E4 W31B	AD9268_D2_P
E5 GND	
E6 W32A	AD9268_D4_N
E7 W32B	AD9268_D4_P
E8 GND	
E9 W33A	AD9268_D6_N
E10 W33B	AD9268_D6_P
E11 GND	
E12 W34A	AD9268_D8_N
E13 W34B	AD9268_D8_P
E14 GND	
E15 W35A	AD9268_D9_N
E16 W35B	AD9268_D9_P
E17 GND	
E18 W36A	AD9268_D11_N
E19 W36B	AD9268_D11_P
E20 GND	
E21 W37A	AD9268_D13_N
E22 W37B	AD9268_D13_P
E23 GND	
E24 W38A	AD9268_D15_N
E25 W38B	AD9268_D15_P
E26 GND	
G1 VIO	FPGA_2.5V
G2 GND	
G3 W47A	AD9781_D12_P
G4 W47B	AD9781_D12_N
G5 GND	
G6 W48A	AD9781_D10_P
G7 W48B	AD9781_D10_N
G8 GND	
G9 W49A	AD9781_D8_P
G10 W49B	AD9781_D8_N
G11 GND	

D19 GND	
D20 W29A	
D21 W29B	
D22 GND	
D23 W30A	
D24 W30B	
D25 GND	
D26 W00D	
F1 GND	
F2 W39A	AD9268_D1_N
F3 W39B	AD9268_D1_P
F4 GND	
F5 W40A	AD9268_D3_N
F6 W40B	AD9268_D3_P
F7 GND	
F8 W41A	AD9268_D5_N
F9 W41B	AD9268_D5_P
F10 GND	
F11 W42A	AD9268_D7_N
F12 W42B	AD9268_D7_P
F13 GND	
F14 W43A	AD9268_DCO_N
F15 W43B	AD9268_DCO_P
F16 GND	
F17 W44A	AD9268_D10_N
F18 W44B	AD9268_D10_P
F19 GND	
F20 W45A	AD9268_D12_N
F21 W45B	AD9268_D12_P
F22 GND	
F23 W46A	AD9268_D14_N
F24 W46B	AD9268_D14_P
F25 GND	
F26 VIO	FPGA_2.5V
H1 GND	
H2 W55A	AD9781_D13_P
H3 W55B	AD9781_D13_N
H4 GND	
H5 W56A	AD9781_D11_P
H6 W56B	AD9781_D11_N
H7 GND	
H8 W57A	AD9781_D9_P
H9 W57B	AD9781_D9_N
H10 GND	
H11 W58A	AD9781_D7_P

G12 W50A	AD9781_D6_P
G13 W50B	AD9781_D6_N
G14 GND	
G15 W51A	AD9781_DCI_P
G16 W51B	AD9781_DCI_N
G17 GND	
G18 W52A	AD9781_D4_P
G19 W52B	AD9781_D4_N
G20 GND	
G21 W53A	AD9781_D2_P
G22 W53B	AD9781_D2_N
G23 GND	
G24 W54A	AD9781_D0_P
G25 W54B	AD9781_D0_N
G26 GND	

H12 W58B	AD9781_D7_N
H13 GND	
H14 W59A	AD9781_DCI_P
H15 W59B	AD9781_DCI_N
H16 GND	
H17 W60A	AD9781_D5_P
H18 W60B	AD9781_D5_N
H19 GND	
H20 W61A	AD9781_D3_P
H21 W61B	AD9781_D3_N
H22 GND	
H23 W62A	AD9781_D1_P
H24 W62B	AD9781_D1_N
H25 GND	
H26 SCLR	FPGA_SCLR

Digital Board Completion